Post-CMOS Packaging Methods for Integrated Biosensors

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Summary

We report on several packaging and integration techniques that have been used in our laboratories for assembling CMOS sensors with secondary structures suited for cell culture and monitoring. All fabrication procedures were conducted post-CMOS and on diced samples. Thus far, two methods have been used for short to medium-term experiments, and one method is currently under investigation for long-term experiments. The first method consisted of micromachining high aspect ratio structures utilizing negative-tone photo-curable resins to simultaneously encapsulate wirebonds and create a cell culture well on the chip's active area[§] (Figure 1). Alternatively, we have pursued a method previously first reported by Martin et al.[**] The authors used an SU-8 structure at the periphery of the active area which acted as a barrier for epoxy that was subsequently flown to encapsulate wirebonds (Figure 2). In our case, we have modified this procedure based on work reported Berdondini et al.[††] to strengthen the adhesion of the SU-8 structure, thereby enhancing the durability of the device. These two methods, although they provide means for testing CMOS chips with cells, exhibit several issues. Notably, the need for high aspect ratio machining in both cases poses significant issues for long term operation, in addition to rendering fabrication procedures difficult. For this reason, we are developing a method which eliminates wirebonding in the immediate vicinity of the chip's active area by extending the chip padframe through a redistribution platform (Figure 3). This effectively reduces the need for high aspect ratio micromachining of encapsulating layers and allows a more planar process to be introduced for passivating the electrical components of the sensor.

Motivations

Packaging is the most important aspect of any sensor system; the sensor's transducer module must adequately interface with the sensing medium without compromising the functioning of other sensor components. In CMOS-based biosensor systems, such as the ones we are developing, a packaging method that allows the introduction of liquid analytes to the sensor surface while maintaining the electrical integrity of the chip is of utmost importance. In addition, the need for such methods is dire for research and development projects where acquiring entire CMOS wafers is cost-prohibitive, and only diced chips are available for prototyping. The methods highlighted herein are expected to adequately address these unmet needs.

Results

Preliminary results have revealed that the micromachining of tall polymer structures in packaged ceramic packages provide adequate encapsulation for up to a week, after which delamination of the structural polymer is observed, and consequently electrical shorting of leads. The second method has shown improved longevity, with successful tests of up to two weeks thus far. The third method is currently being further developed and tested.

[§] R, Delille, M. Urdaneta, S. Moseley, and E. Smela, *J. Microelectromech. Syst.*, 15 (5), 2006, pp. 1108-1120.

[**] S. M. Martin, T. D. Strong, and R. B. Brown, *Proc. Intl. Conf. MEMS, NANO, and Smart Systems*, 2004.

[††] L. Berdondini, M. Chiappalone, P.D. van der Wal. et al., *Sens. Actuator B-Chem.*, 114, 2006, pp. 530-541.

Figures

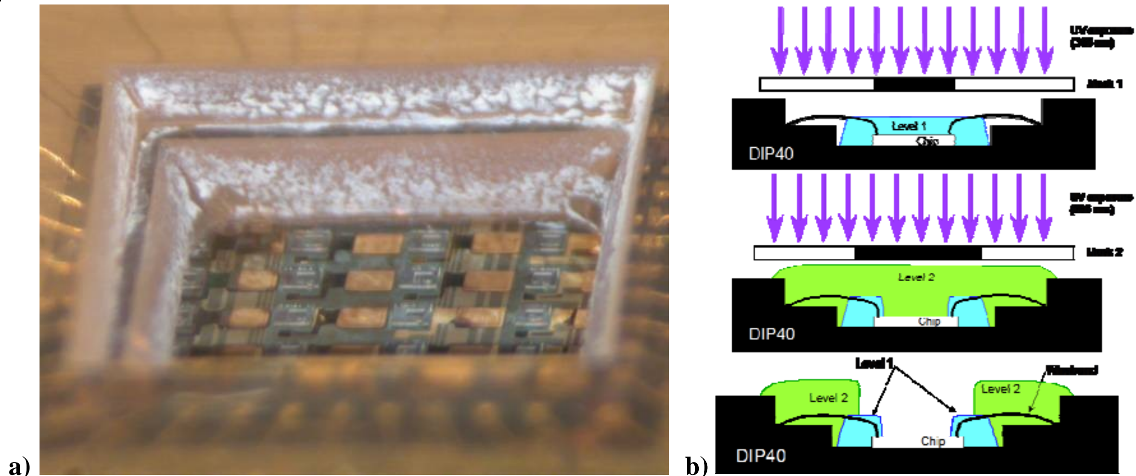

Figure 1. a) Chip mounted in DIP40 package with encapsulated wirebonds. b) Summary of the fabrication procedure used for encapsulating the packaged chip.

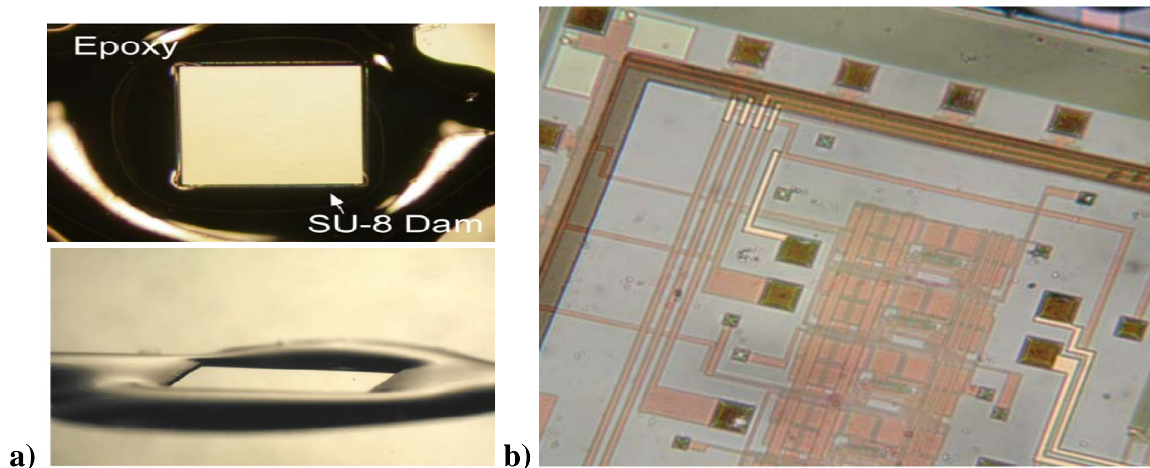

Figure 2. a) Method showing SU-8 dam with back-flowed epoxy for encapsulating wirebonds. b) Photomicrograph of a CMOS chip (with electrolessly plated Au pads and electrodes) on which the SU-8 dam was micromachined.

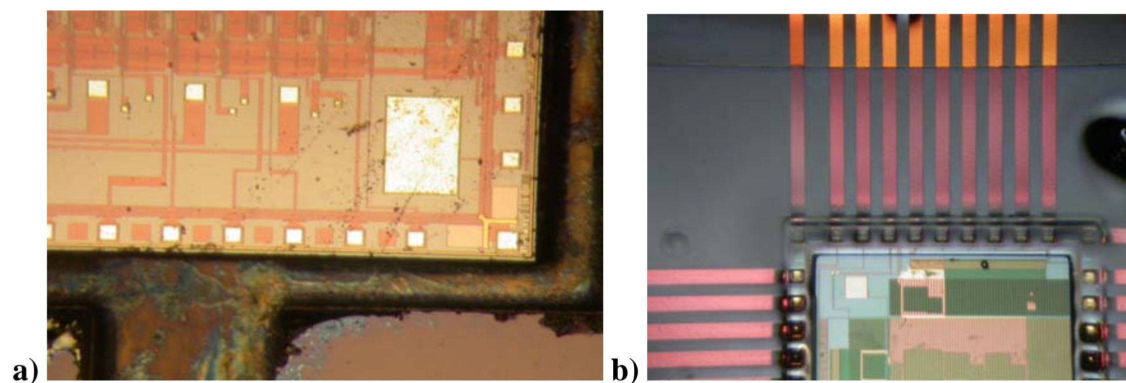

Figure 3. a) Chip placed within a redistribution platform for extending the padframe further away from the chip's edge. The chip is mounted in a cavity in which epoxy can be flowed around it to ensure planarity. b) Chip mounted in a cavity, with surface metalized and then encapsulated.